



AUCOTEC
Create Synergy – Connect Processes

RUPLAN EVU-Module

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1 Object editing

1.1 Evaluations

Funct. object: enter U&, V&

New feature

The automatic entry at a circuit diagram symbol of "V&TX4" into the text node 'TX4' from now on is only performed if the text node has been empty before.

2 Sheet editing

2.1 Toolbars and icons

DIN only: Toolbar "Circuit diagram" / "Frames, groups, tables" / "Circuit paths / frames" / 3 features to enter a location or an item polygon

Fixed bug

When entering a location or an item polygon, occasionally the group corner symbols (GJ512 for a location polygon, GJ505 for an item polygon) were entered in a faulty angle.

Toolbar "Circuit diagram" / "Wiring" / " Wiring order" / "Wiring editor"

Fixed bugs

- The sheet number (system variable) was carried along with only 4 digits. Thus, in big projects, sheets with 5-digit sheet numbers were not correctly processed.
- The cable core entry of an external connector had been written into the column "pin".

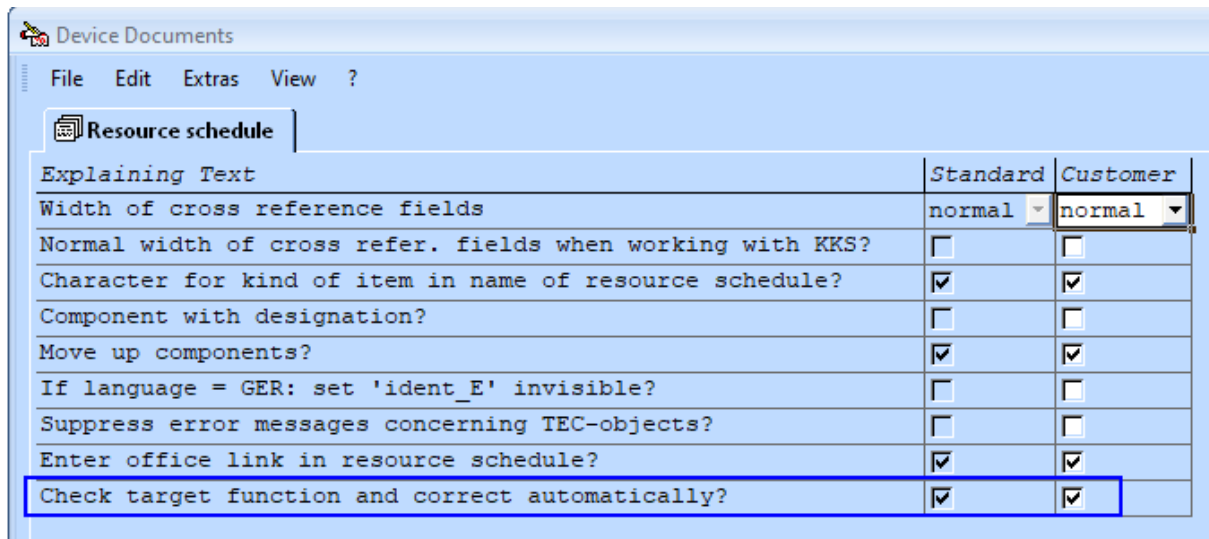
3 Evaluations

3.1 General

3.1.1 Project settings

3.1.1.1 NEW: Switch off auto-correction of the target function with the resource schedule

The automatic correction of the target function entry at the start of the resource schedule (resp. terminal function diagram in IEC-projects) was hard-coded. Now it can be switched off:



See also chapter 3.4.1, Create resource schedules / Create terminal function dgr.

3.2 Menu "General diagram processing"

3.2.1 Main menu

Check title block inscription

New feature

The checks got an error code at the end of the line. The de-coding for the error code is listed in the error list header.

Example from a DIN-project:

In the diagrams listed below at least one of the following errors has occurred:

- => 1. The entries of "ZTEIL" do not correspond with the RUPLAN address (sheet designation).
- => 2. The text field "=" has no entry.
- => 3. The text field "UART" (document type) has no text.
- => 4. The symbol type (S&ART) is faulty.
- => 5. Wiring material information is missing at the title block of a circuit diagram.

| Function | Address | ZTEIL | RMAT / S&ART | UART | RMAT / S&ART | RQUER | RFARBE | Error |
|----------|---------|-------|--------------|------|--------------|--------|--------|-------|
| =E02 | A00 | A00 | | A | | | | 2 |
| =E02 | Q01 | Q01 | =E02 | | H07V-K | 1,5mm2 | BK | 3 |
| =E02+S1 | Q01 | Q1 | =E12 | V | H07V-K | 1,5mm2 | BK | 1 |

Copy sheets, bay-related

Fixed bug

If, by copying a bay from a read-only sheet library, sheets in the first sheet library were overwritten, this could result in corrupt sheets.

Therefore, the copying from a read-only library is now only allowed if no sheets with the same name exist in the 1st sheet library.

3.3 Menu "Circuit diagram commands"

3.3.1 Submenu "Connections and connectors"

Start wiring editor

New feature

If a cross-connection contains wiring symbols, it no longer is displayed by the wiring editor: Mixing these two ways of laying down the wiring order is not allowed.

Fixed bug

The sheet number (system variable) was carried along with only 4 digits. Thus, in big projects, sheets with 5-digit sheet numbers were not correctly processed.

3.3.2 Submenu "Wiring material"

3.3.2.1 Equalize wiring mat. spellings

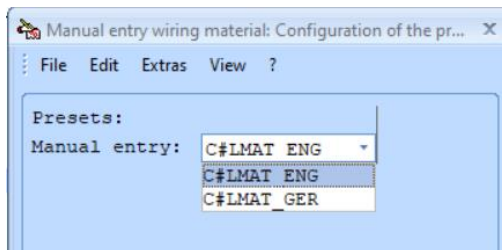
Only the blocks that must be equalized are shown, making the entry mask easier to survey.

3.3.2.1 NEW: Configuration of the presets for manual entry of w-mat

If for assigning wiring material the option "Manual entry" is chosen, in the 3 text nodes for the complete wiring information, presets for common values are offered.

These offerings can be adapted.

After the start of the evaluation, the user is asked which language-related address should be changed:



The content of the chosen address is offered for changes:

| ID | No | Value | Category | |
|----|--------|-------|-------------|---------------|
| S0 | S1 | S2 | S3 | S4 |
| 2 | C&_LMT | 01 | H07V-K | Wire type |
| 3 | C&_LMT | 02 | H07Z-V | Wire type |
| 4 | C&_LMT | 03 | H05V-K | Wire type |
| 5 | C&_LMT | 04 | YV1 | Wire type |
| 6 | C&_LMT | 05 | FBST500-PLC | Wire type |
| 7 | C&_LMT | 06 | BB-jumper | Wire type |
| 8 | | | | |
| 9 | C&_LQT | 01 | 0,75mm² | Cross Section |
| 10 | C&_LQT | 02 | 0,8mm² | Cross Section |
| 11 | C&_LQT | 03 | 1,5mm² | Cross Section |

Permissible are:

- Changing entries
- Deleting lines
- Duplicating lines



The changes will only be valid after leaving and re-entering the project.

3.3.2.2 Submenu "Conversion to new workflow"

Switch: pos. to material

Change

When converting the project, the old standard material from the wiring material table header should be installed at the standard for the project in the project settings.

The window with alternatives is therefor no longer displayed.

3.4 Menu "Device documents"

3.4.1 Create resource schedules / Create terminal function dgr.

New feature: Auto-correction of the target function can be switched off

When starting Create resource schedule / Create terminal function diagram, a target function can be entered in each parameter line. Subsequently, these entries are checked according to certain rules, and are corrected in case of deviations.

This can lead to the effect that a desired target function has to be entered several times. For this reason, it is now possible to switch off the auto-correction functionality.

Switching off (and switching on again) is done via the project setting; see chapter 3.1.1.1, NEW: Switch off auto-correction of the target function with the resource schedule.

3.5 Menu "Terminal diagram"

3.5.1 Main menu

3.5.1.1 Create terminal diagram

New feature:

Targets in the terminal diagram can be set invisible by means of special accessories symbols EXXU*. This possibility was created to set targets on the same terminal strip invisible if they are displayed graphically by an insertable jumper.

If by this means a target that is not part of the terminal strip is set invisible, then this is normally not wanted. Therefor, these cases are entered into the error list:

```
=E01+KF01-X1          119      : target 1 is no terminal of this terminal block, but it is invisible.
```

Fixed bugs:

If no optional wiring material table is used, the position numbers for differing wiring material in the terminal block diagram header are just counted upwards. With this counting, gaps occurred.

3.5.1.2 NEW: Data transfer wiring material special TDR -CDR

New feature

This evaluation transfers wiring material entries from the terminal diagrams to the circuit diagrams.

Herewith, it examines targets of a terminal. These targets are now found sheet-overlapping as well.

3.5.1.3 NEW: Data transfer from CCD/WL

New feature

This evaluation transfers wiring material entries from the cross-connection diagrams or the wiring lists to the circuit diagrams.

Herewith, it examines the neighboring targets of each participant of a cross connection. These targets are now found sheet-overlapping as well.

3.6 Menu "Cable documents"

3.6.1 Cable definition sheets / cable list

Fixed bug

For error messages with a navigation possibility to the cable definition sheets / cable overview plans, the evaluation aborted because the navigation data pointed to a sheet that had been temporarily created and already deleted at the time of the error display.

3.6.2 Cable connection diagram

Fixed bug

IEC only: If in an IEC project the setting sheet for DIN projects was active, the cable connection diagram aborted. Now, in this case the following message is displayed: "The setting sheet could not be read correctly. Please check: VDR KA2".

3.7 Menu "Wiring diagrams"

3.7.1 Cross connection diagram

Fixed bug

Continuing a cross-connection on a new sheet was not marked reliably.

3.7.2 NEW: Data transfer from CCD/WL

New feature

This evaluation transfers wiring material entries from the cross-connection diagrams or the wiring lists to the circuit diagrams.

Herewith, it examines the neighboring targets of each participant of a cross connection. These targets are now found sheet-overlapping as well.

3.7.3 Device wiring list / Device connection list

Fixed bug

IEC only: If the RUPLAN-function of the circuit diagram consisted of only one character (e.g. "-"), then no target function was created, and the evaluation aborted.

3.7.4 Plug connection diagram

Fixed bug

If in the form sheet lines were missing for pins in the circuit diagram, no error message was displayed. – The new error message was integrated in "Create plug connection dgr." as well as in "Create plug conn. dgr. (int.)".

3.8 Menu "Derived documents generator"

FoDoG: settings

New feature

If you start the FoDoG-settings, now the project setting mask is positioned straight to the **FoDoG**-tab, no matter what tab had been active before.

4 QS-tools

4.1 Connections and potentials

4.1.1 Connection check

New: Consistency wire cores ↔ connections is checked

Wiring material information at wire cores are checked against the material information at the adjoining connections:

| | | | |
|------------------------------|--|----------------------------|--------------------------------|
| Project: STUW45641_U2_TEST_2 | | User: BNO | |
| Date: 02.11.2021 | | Page: 1 | |
| ----- | | ----- | |
| Check: | Connection check | Result: | Incorrect |
| ----- | | | |
| Error: | 1: The connection has at least one open end. 2: The length of the connection is smaller than 4 mm. 3: The open end of the connection borders free graphics. 4: The network text is placed outside of the grafical area. 5: Drahtaderbeschriftung stimmt nicht mit Leitungsmaterial überein | | |
| ----- | | | |
| Search Terms | | | #Error |
| Function | Sheet | Network Name | X Y X1 Y1 X2 Y2 V&INDEX |
| | | Leitungsmaterial Drahtader | Leitungsmaterial Verbindung |
| | | | # 1 2 3 4 5 |
| =ET05 | R02 | H07V-K | 1.5MM2 SW H05V-K 1.0MM2 SW # X |
| ----- | | | |

5 Export Multipage PDF

Short description

In the 1st sheet library of a project, a multipage PDF file can be generated for a marked selection of sheet. The menu for the export-settings and the export itself can be reached via the pull-down menu **Output**.

Further new features

Export from IEC-projects available

The export of IEC projects via MPP with navigation was made suitable for running; especially the trees were straightened out.

Cable core lines in the cable connection diagram

With the MPP export with navigation, now navigation is possible from the cable cores in the cable tree to the core lines in the cable connection diagram.

Fixed bug

Device pins (GER and STE) in the tree structure were missing

- Multipage-PDF export with navigation: In the tree, pins of devices of the object class GER were missing. The object class STE was missing completely.
- Form sheets (functions VDR*) are excluded from the export; they could cause trouble if they content item designation (form sheets for formatted terminal diagrams).

6 EVU Viewer (International)

Fixed bug

For working in the Viewer, the online processing is disabled. That lead to the effect that functions with read-only access to B records aborted. This applied especially to the navigation.